Methodology for Retention Lifetime Estimation and Activation Energy Calculation in PermSRAM® Technology

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Retention lifetime is a major issue when developing non-volatile memories using a new mechanism. PermSRAM® technology utilizes hot-carrier effects to program. The generated electrons are mainly trapped in the Si_3N_4 layer in the sidewall spacer. In non-volatile memories using trapping mechanism, including SONOS, it is known that the Poole-Frenkel current dominates the de-trapping and determine the lifetime [1, 2]. This paper describes the methodology of retention lifetime estimation and activation energy calculation for memory cells in PermSRAM technology from NSCore. In this methodology, we consider statistical variation to predict lifetime in different temperatures. When we set our design criteria, we assume the cell failure rate is less than 1ppb, which is equivalent to 100ppm for a 100-Kb memory macro.

Figure 1 shows the cumulative plot of the cell currents for 128 cell transistors after program and bake for up to 30 hours at 200°C, as well as initial cell currents. The horizontal axis is cell current and the vertical axis is multiples of standard deviation (s). The data shows that all the currents have normal distribution even after program and bake. To guarantee the cell failure rate is less than 1ppb, we have to consider the worst case in approximately 1-Gb cells, which is equivalent to +/- 4σ variation. We set our criteria for retention lifetime as the bake time when +4 σ of current distribution after bake reaches to 90% of -4 σ of initial current distribution. In our design, the sense amplifier can correctly sense if the ratio of programmed current to initial current is 90% or less.

Figure 2 shows +4 σ of the cell current distribution as a function of bake time. The data shows the +4 σ of the cell current distribution is proportional to the logarithm of the bake time. This relationship is very similar to the relationship between hot-carrier degradation and stress time. The cross point of the +4 σ of the cell current distribution and the line at ID = 90% × (-4 σ of initial current distribution) is the retention lifetime of the devices. We then take retention characteristics in different temperatures and draw the same graphs as shown in Fig. 3. The retention lifetime decreases as the bake temperature increases.

The relationship between lifetime and baking temperature is determined by the Arrhenius equation,

$$\text{Lifetime} = A \cdot \exp(Ea/kT) \qquad (1)$$

where 'Ea' is activation energy, 'A' is a constant, 'k' is Boltzman constant, and 'T' is absolute

temperature.

The lifetimes obtained from Fig. 3 can be plotted on the Arrhenius plot shown in Fig. 4. This graph can give lifetimes at different temperatures as well as activation energy from the Eq. 1.

This document addresses only the methodology to predict retention lifetime in operation temperature. Please refer to the qualification report for each of the processes to know the actual lifetime and activation energy.

References

[1] S. Kumar, and E. L. Russel, “Model to predict ONO non-volatile memory”, *Integrated Reliability Workshop (IRW)*, pp. 34-40, 2001.

[2] Hang-Ting Lue et al., ”Reliability Model of Bandgap Engineered SONOS(BE-SONOS)”, *IEDM Technical Digest*, pp. 495-498, 2006

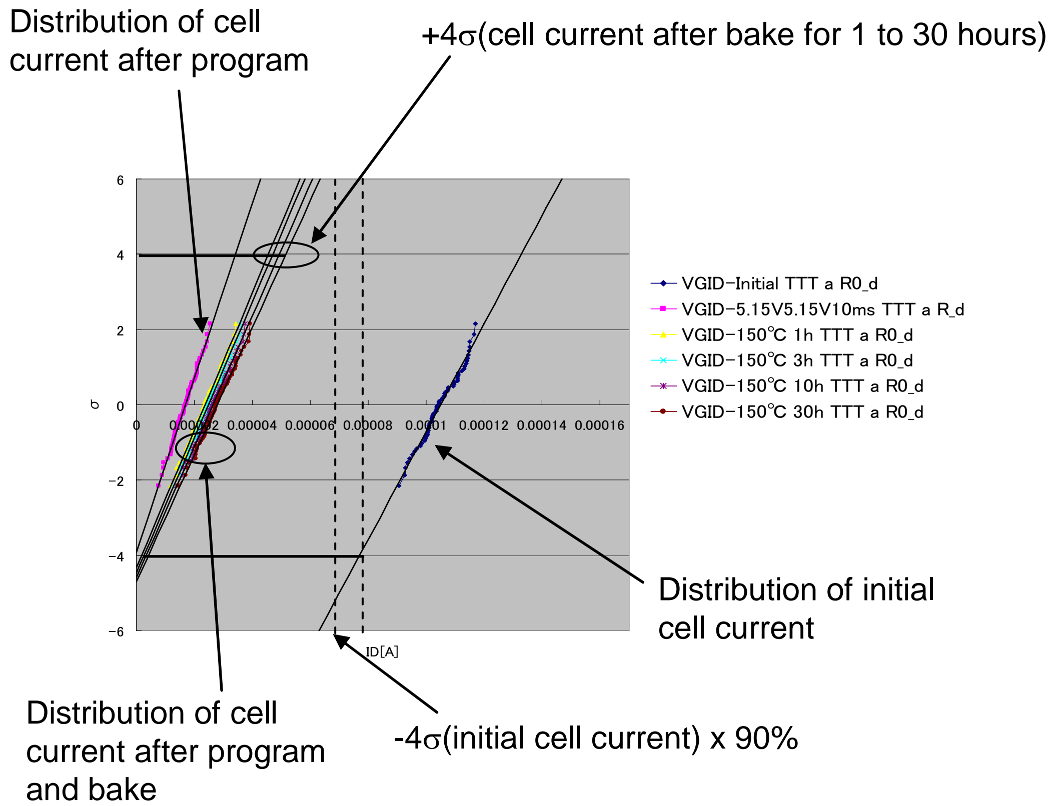


Fig. 1

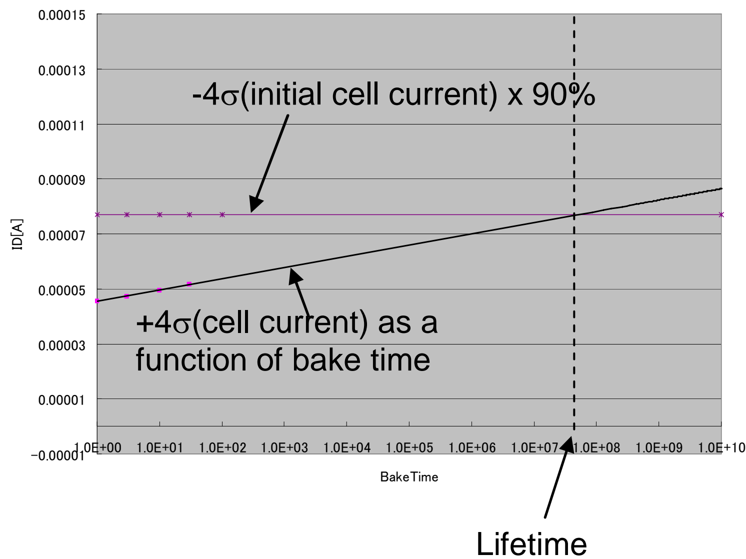
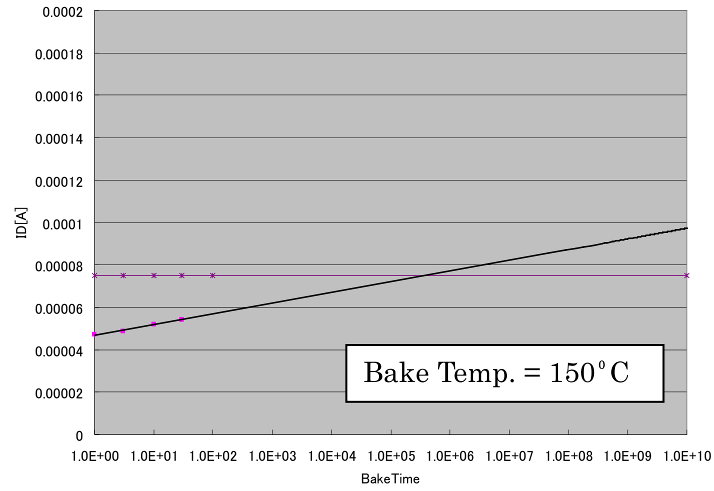
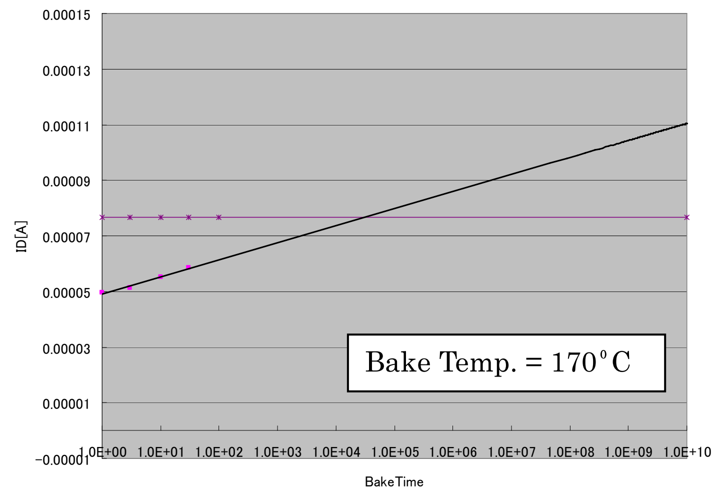


Fig. 2





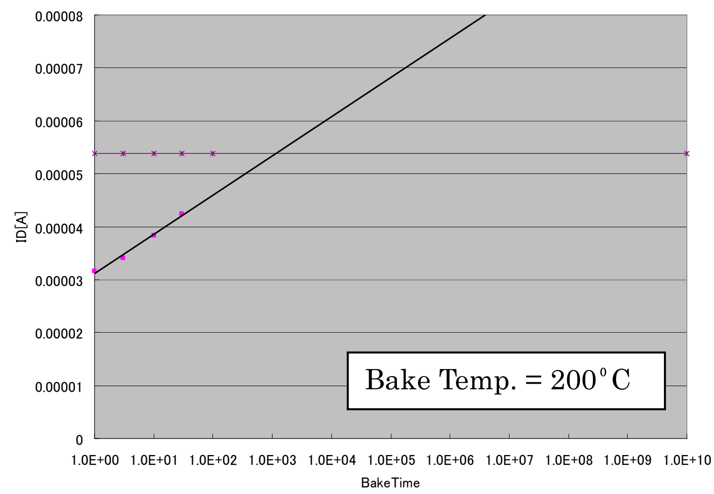


Fig. 3

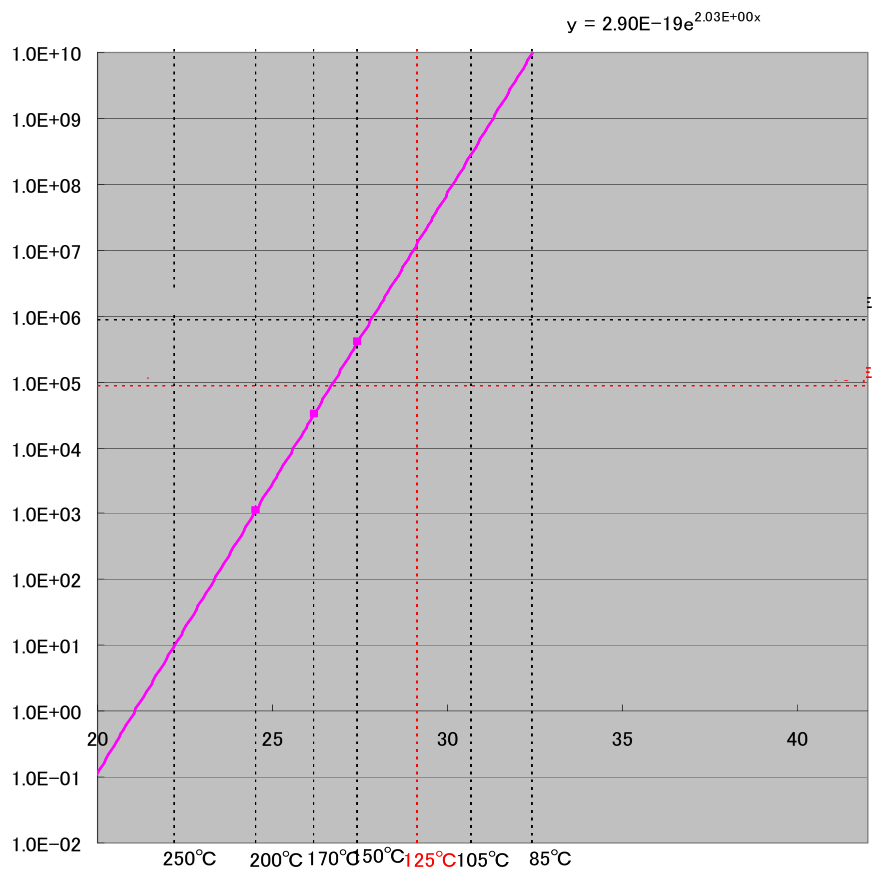


Fig. 4